REMARKS

This amendment responds to the first office action. Claims 19-20 and 65-66 have been amended, and new claims 71-79 have been added.

The Examiner has requested that applicants update the status of the parent application. Applicants note that the parent application Serial No. 07/389,334 has issued as U.S. Pat. No. 5,440,749. Also pursuant to the Examiner's request, a new title and new abstract more aptly descriptive of the invention have been provided.

The Examiner has rejected claims 19-21 and 65-67 under 35 U.S.C. § 112 as being indefinite. With respect to the apparatus claims, the Examiner asserted that there exists no functional relationship and interconnection between the claimed components. Similarly, the Examiner asserted that a functional relationship does not exist between the steps of the method claims, and that it is unclear what the steps try to accomplish.

Applicants note that the present invention is directed to a microprocessor system including a central processing unit and a ring oscillator variable speed system clock connected thereto. In accordance with the claimed invention, the central processing unit and the ring oscillator variable speed system clock are provided in a single integrated circuit. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. By this amendment the term "ring counter" has been replaced with "ring oscillator", in order to more particularly identify the ring oscillator (FIG. 18) incorporated within a preferred implementation of the microprocessor system of the invention.

Although applicants submit that the "functional relationship" between the claimed central processing unit and system clock connected thereto is inherently clear, the apparatus and method claims have been amended in an effort to accommodate the Examiner's concerns with respect to 35 U.S.C. §112. For example, claim 19 now recites a "functional relationship" in that it is made explicit that the ring oscillator variable speed system clock is disposed to clock the central processing unit. Moreover, the central processing unit and ring oscillator variable speed system clock are described as "each including a plurality of electronic devices of like type". This allows the central processing unit to operate at a

variable processing frequency which depends upon a variable speed of the ring oscillator variable speed system clock. See, for example, the specification at page 31, line 33 to page 32, line 1:

> By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 *ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates*, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

Method claim 65 has been similarly amended, and now recites the step of:

> fabricating a ring oscillator system clock having a plurality of transistors, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor ... .

The method claims thus now prescribe a technique for clocking a microprocessor using a ring oscillator system clock comprised of transistors having similar operating characteristics as those within the microprocessor. This advantageously allows the processing frequency of the microprocessor to track the clock rate of the ring oscillator system clock.

The Examiner has rejected claims 19 and 65 under 35 U.S.C. § 103 as being unpatentable over Sheets. The Examiner stated that Sheets teaches a microprocessor system having a microprocessor and a variable speed clock generator. Although admitting that Sheets does not disclose that his clock is implemented using a ring oscillator, the Examiner opined that a "counter is a basis component of [a] clock generator". It was further asserted that choosing the counter to be of the ring type is merely a matter of design choice.

Applicants again observe that the present invention is directed to a system and method for clocking a central processing unit disposed *within the same integrated circuit* as a ring oscillator variable speed system clock. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. That is, the operational speed of the microprocessor and ring oscillator clock are designed to vary similarly as a function of variation in temperature, processing and other parameters affecting circuit performance.

The system of Sheets effects microprocessor clocking in a way which is entirely dissimilar from that of the present invention, and in fact teaches away from Applicants' clocking scheme. In particular, Sheets describes the use of discrete, commercially available microprocessor chips, e.g., the Motorola 68000 (col. 5, line 16), driven by a separate clock (VCO 12 of FIG. 1). As is well known, such microprocessor chips include terminals or pins, such as the CLK and INT terminals of microprocessor (FIG. 1), for receiving inputs from external devices like the VCO 12 and fixed oscillator 103. Because the VCO 12 is not integral with the microprocessor 101, Sheets has proposed a technique for adjusting the frequency of VCO 12 in accordance with a desired operating frequency of the microprocessor 101. Specifically, a digital word indicative of this desired operating frequency is written by microprocessor 101 to VCO 12 by way of data bus 104 as a means of adjusting clock frequency.

The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance. Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

Although the foregoing clearly indicates the existence of a patentable distinction between the system of Sheets and the present invention, claims 19 and 65 have nonetheless been amended to advance prosecution of the application. Specifically, claims 19 and 65 now explicitly recite that the ring oscillator and microprocessor are provided within the same integrated circuit. Moreover, these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock:

...The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process.
(page 32, lines 10-13)

Neither of these aspects of the present invention are suggested by Sheets. As discussed above, Sheets describes the use of commercially available microprocessor chips, and depicts the microprocessor 101 as being coupled to a separate clock (i.e, VCO 12) by way of a data bus 104 and address bus 105. Moreover, the VCO 12 clearly is not comprised of transistors having operating characteristics disposed to vary similarly to those of transistors within the microprocessor 101. Rather, the VCO 12 is seen to be comprised of an LC oscillator (col. 3, line 58 and FIG. 6), which clearly is not adapted to mimic variation in the speed of transistors within the microprocessor 101. Accordingly, applicant respectfully submits that amended claims 19 and 65 are patentable over Sheets, and requests that the rejection thereof under 35 U.S.C. § 103 be withdrawn.

Since Schaire does not supplement the lack of teaching within Sheets with respect to amended claims 19 and 65, it is also respectfully submitted that pending claims 20-21 and 66-67 are patentable over Sheets in view of Schaire. Further with regard to pending claims 20 and 66, it is observed that Schaire provides no indication that bus interface unit 10 is clocked by a signal from a clock different from that used to clock the host microprocessor. That is, the origin of high-speed clock signal 230 (FIG. 1) provided to bus interface unit 10 does not appear to be described. Hence, Schaire fails to teach the claimed provision of separate, independent clock signals to an input/output interface buffer and microprocessor. Accordingly, applicant respectfully requests that the outstanding rejection of claims 20-21 and 66-67 under 35 U.S.C. § 103 be withdrawn.

By this amendment new claims 71-79 have also been added to more particularly identify the invention which appears to be available for protection. In this regard new claims 71-72 point out that information is transferred to and from the microprocessor in synchrony with the ring oscillator system clock, and that this information is buffered to facilitate transfer thereof to and from system memory synchronously with respect to the ring oscillator system clock. New claims 73-79 explicitly recite that the central processing unit and ring oscillator include first and second pluralities of transistors, respectively, and that the

operating characteristics of these transistors vary in the same way as a function of variation in operational parameters (e.g., operating temperature) of the substrate. This advantageously allows a processing frequency of the central processing unit to track a clock rate of the ring oscillator as a function of substrate parameter variation.

Accordingly, in view of the above remarks, it is submitted that this application is now ready for allowance. Early notice to this effect is solicited.

If in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned at (415) 843-5000.

Respectfully submitted,

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